**Computer Hardware Experiments**

Lab\_03: Digital Display and Gray Codes

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1. The VHDL source code：

-----------------------------------------------------------------------------

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity led is

Port ( B : in STD\_LOGIC\_VECTOR (3 downto 0);

L : out STD\_LOGIC\_VECTOR (6 downto 0));

end led;

architecture Behavioral of led is

begin

L <= "1011111" when (B = "0000") else

"0000011" when (B = "0001") else

"1110110" when (B = "0010") else

"1110011" when (B = "0011") else

"0101011" when (B = "0100") else

"1111001" when (B = "0101") else

"1111101" when (B = "0110") else

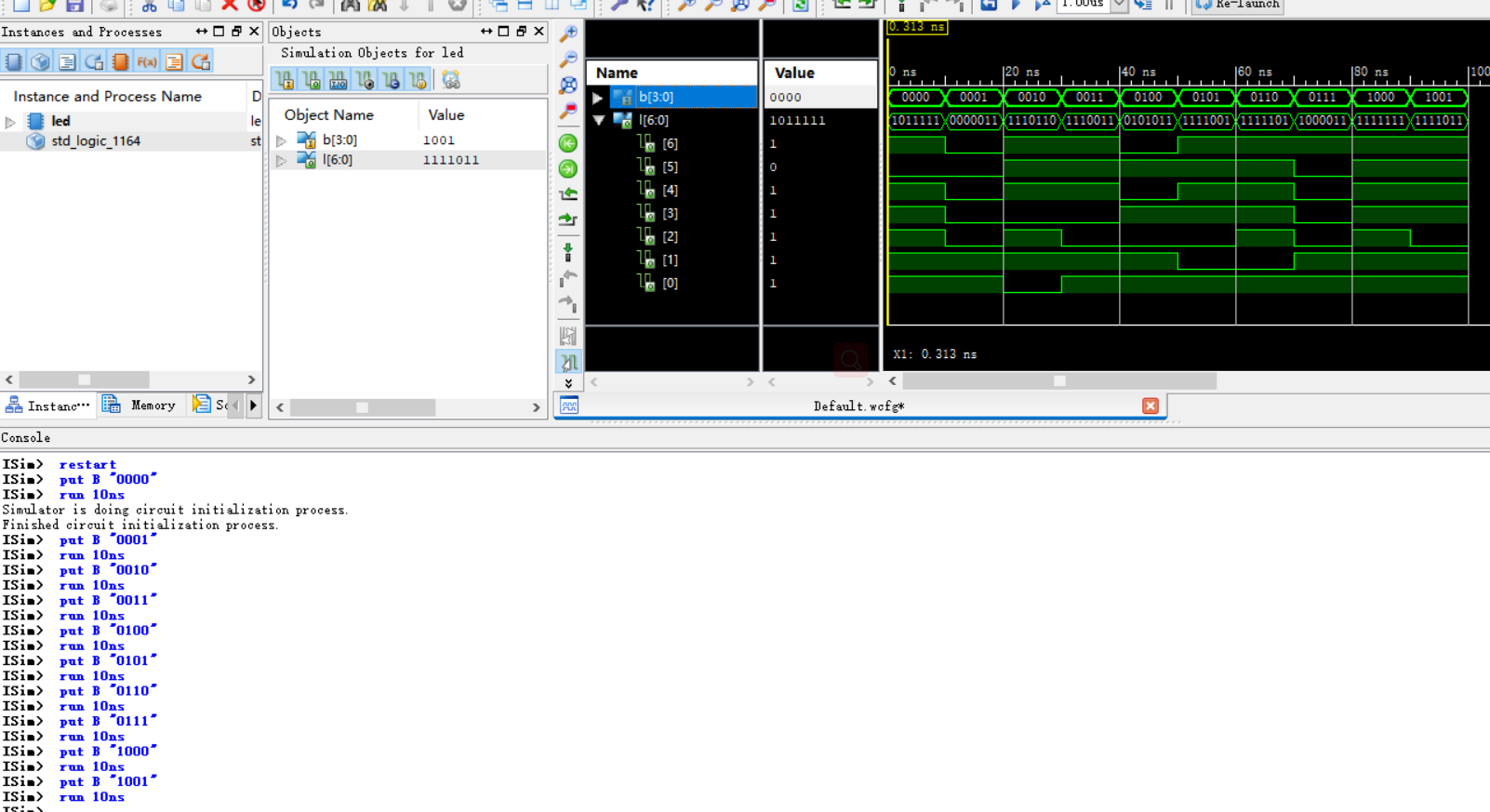
"1000011" when (B = "0111") else

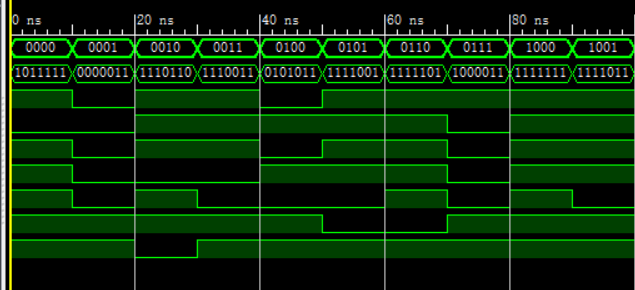
"1111111" when (B = "1000") else

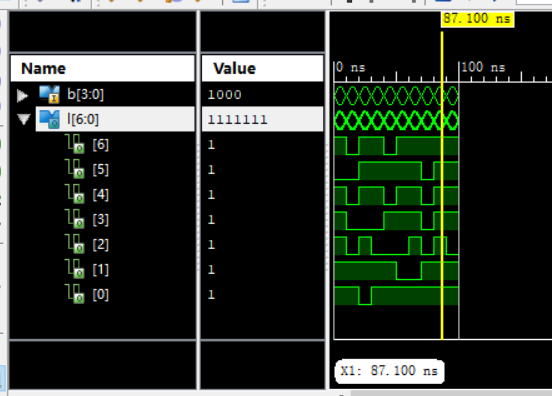
"1111011";

end Behavioral;

The simulation waveform：







1. GaryDecode:

The VHDL source code：

----------------------------------------------------------------------------------------------------------------------library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use ieee.std\_logic\_arith.all;

use ieee.std\_logic\_unsigned.all;

use ieee.numeric\_std.all;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity decoder is

Port ( BinaryNum : out bit\_vector (3 downto 0);

GrayNum : in bit\_vector (3 downto 0));

end decoder;

architecture Behavioral of decoder is

signal tmp1 : bit\_vector(3 downto 0);

signal tmp2 : bit\_vector(3 downto 0);

begin

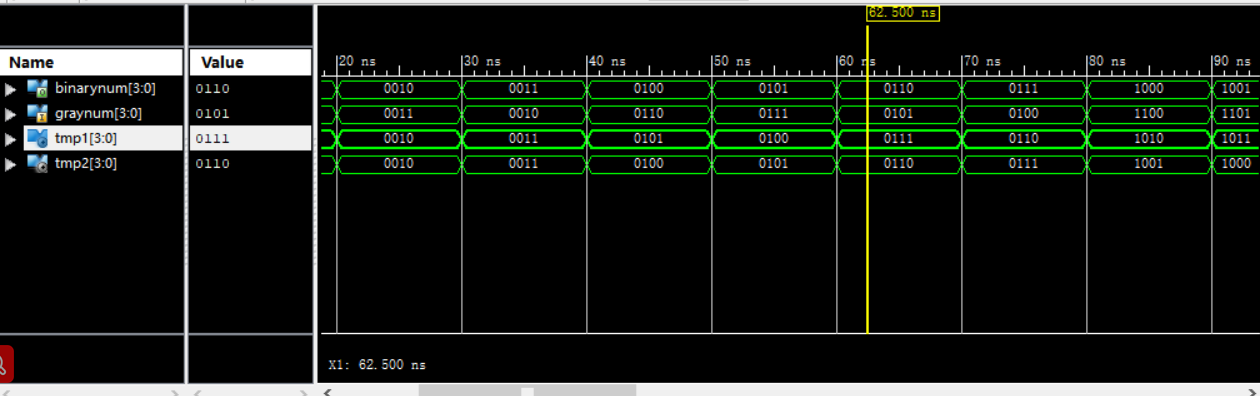
tmp1 <= (GrayNum srl 1) xor GrayNum;

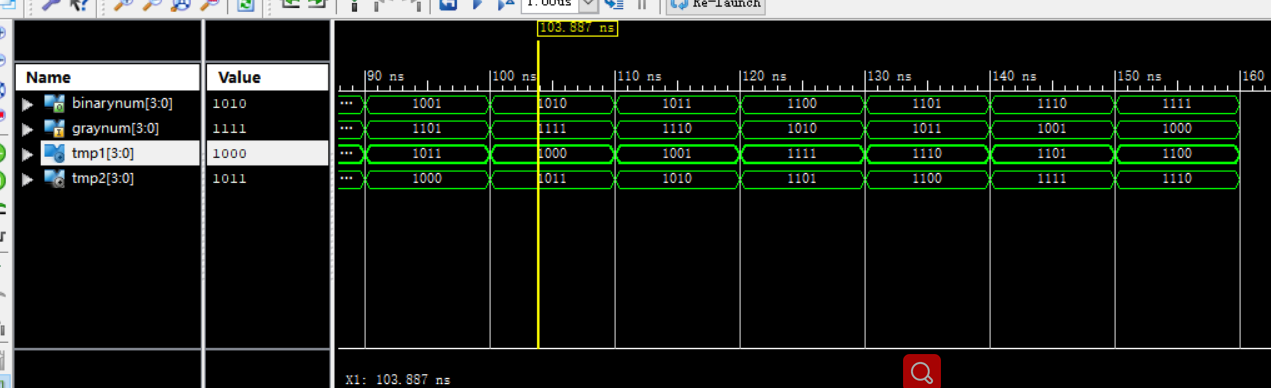
tmp2 <= tmp1 xor (GrayNum srl 2);

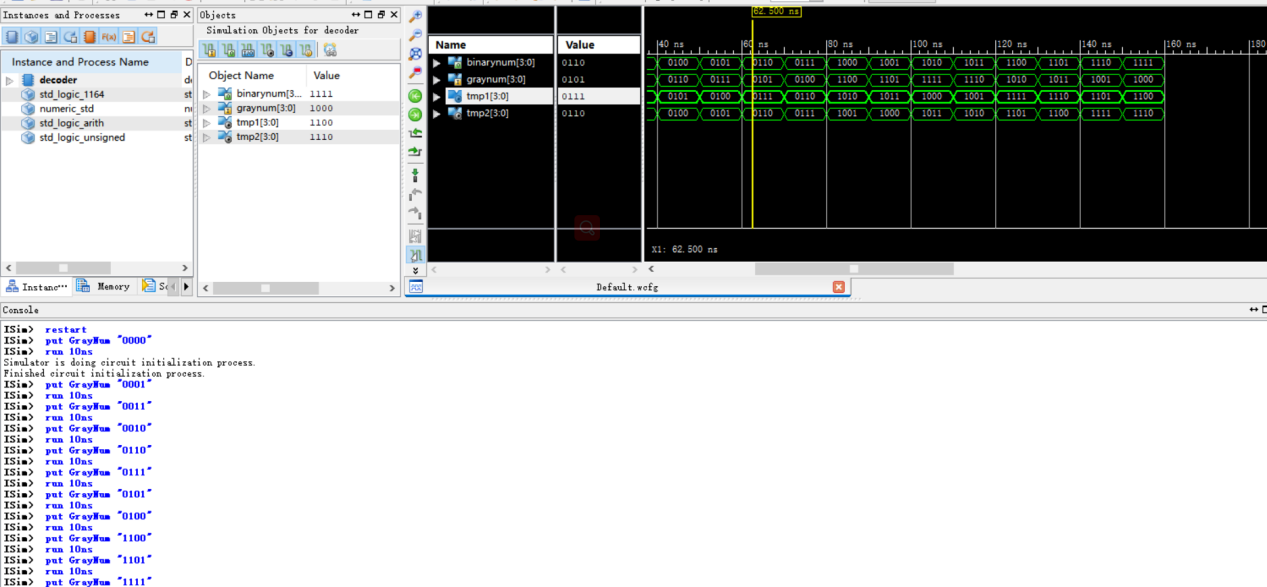
BinaryNum <= tmp2 xor (GrayNum srl 3);

end Behavioral;

The simulation waveform：







GaryEncode:

The VHDL source code：

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use ieee.std\_logic\_arith.all;

use ieee.std\_logic\_unsigned.all;

use ieee.numeric\_std.all;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx primitives in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

entity encoder is

Port ( B : in STD\_LOGIC\_VECTOR (3 downto 0);

G : out STD\_LOGIC\_VECTOR (3 downto 0));

end encoder;

architecture Behavioral of encoder is

signal T: STD\_LOGIC\_VECTOR (3 downto 0);

begin

T(2 downto 0) <= B(3 downto 1);

T(3) <= '0';

G <= B xor T;

end Behavioral;

The simulation waveform：

